Summary of FPHX-V2 review, Sept 29, 2008

Reviewers: John Haggerty, Cheng-Yi Chi, Mike Leitch, Eric Mannel

Summary of presentations:

A total of 5 presentations were presented at the review:

1. S. Butsyk: FVTX Electronics System Design
2. J. Kapustinsky: FPHX Design Overview and Analog Test Results
3. P. McGaughey: FPHX Digital and Real Data Test results
4. M. Brooks: Production Quantity FPHX Chips

The first (S. Butsyk) talk provided an overview of the electronics used to test the FPHX-V2 chip, along with some of the testing that was done to verify that the chip worked from a digital standpoint. In varying configurations, FPHX-1 and FPHX-2 chips have been mounted to a PCB and Kapton versions of the HDI and wire bonded to prototype strip sensors.

Results of calibrating 13 chips on a Kapton HDI were presented. The effects of the different strip capacitance due to the sensor geometry were evident. It was noted that the FPHX chip has the ability to compensate for this, but that was not done for this calibration run.

Results of source testing were also shown. It was noted that the data were taken untriggered and so the discriminator threshold was set a factor of 2 higher then what is anticipated for in the normal operation of the detector.

HDI stress testing has been preformed on a Kapton HDI with 15 chips. No problems were observed with the BCO clock operating as low as 4/5 of the nominal 10MHz. Problems started to appear when the BCO clock was operating at 5.5/5 the nominal 10MHz. It was stated that the ROC FPGA design may be the limiting factor, and that there is at least a 10% safety factor in terms of the read clock. Studies were also done on looking at the reset w.r.t the BCO, looking at the effect of the read clock phase with respect to the BCO and looking at the response to long sequences of well spaced pulses. No quantitative results were presented on these studies.

The second talk (J. Kapustinsky) reported on the initial testing of the FPHX-1 chip, design changes in the FPHX-2 chip, results of testing the FPHX-2 chip and plans for Q/A testing of the chip. The results of the FPHX-1 chip have been reported in previous reviews, so are not commented on here. There were several design changes in the FPHX-2 chip. These included setting the proper W/L for all input transistors, increasing the BCO counter 1 bit, reducing the threshold dispersion, and fixing the “Freeze-Frame” problem for large hit events. Studies done on the FPHX-2 chip indicate that the W/L of the input transistor has been properly for the desired chip response. Studies of the threshold dispersion show that the dispersion has been reduced ~50% with respect to the

FPHX-1 chip. In addition, design changes in the analog front end have increased the number of gain settings that can be programmed. Results were shown that the new gain settings are working as desired.

Modifications to the digital backend, addition of 7^{th} BCO bit, enabling readout through serial 1, serial 2 or both, and correction of the "Freeze-Frame" have also been implemented and the results of the tests provided.

Preliminary plans for testing of the die have started and this will be done at FNAL. Work has already started to assemble the required software and hardware to do the testing. Member of the FVTX group will assist the FNAL testing team, headed by A. Baumbaugh in designing the testing software and outlining what tests need to be done.

The third talk (P. McGaughey) discussed additional digital, cosmic ray and beam testing. The conclusions of a number of tests that were suggested at the FPHX-1 review were given and no issues have been observed that would prevent going forward with the current design.

Results of the tests to verify the "Freeze-Frame" correction, and threshold dispersion corrections were shown, along with the result of injecting very large signals into the front end of the chip. These results support that the "Freeze-Frame" problem has been corrected and threshold dispersion reduced. The results of the large amplitude analog signals show that the analog front end is very robust.

Plots showing the effect on the ADC output due to the timing of the inject pulse with respect to the BCO were also shown. For some timing widows, the ADC response varies from what is expected. Namely for certain timing windows and inject pulse amplitudes, the ADC output can be 0, and not the expected value of 3 or 4. It was pointed out that there is a time window of ~50ns for which this effect is not seen. Considerable discussion was focused on this issue with a description of what could lead to this effect from J. Hoff, the design engineer. The explanation is that the timing of the comparator crossover is not the same for all comparators, that is, low threshold comparators will trigger before high threshold comparators. If the timing is such that the ADC readout occurs as the time the comparators are triggering, then one can get an unexpected ADC value. These results from the asynchronous timing of the inject pulse with respect to the BCO. If one can set the timing properly, this should not be an issue. There was discussion of what the possible timing dispersion could be over the entire FVTX system and if the ± 20 ns window would be sufficient. The conclusion was that it should be, but careful consideration should be paid to the clock dispersion for the system.

Results of some cosmic ray data taking were also presented. Studies of efficiency looking at tracks passing through 4 planes of detector give a lower limit of 97% for tracking efficiency. The mean charge collected is ~23K electrons, which is consistent with the expected charge deposition for the silicon sensor. Both FPHX-1 and FPHX-2 chips have equivalent performance.

Results of the beam test performed at LANCE were also shown. Due to the nature of the beam, the multiplicity was high, making it difficult to carry out detailed analysis of the data. However, under these conditions, the detector and readout worked correctly.

The final presentation (M, Brooks) was over cost and schedule. This covered not only the schedule for the FPHX engineering run, but other components required to build the FVTX wedges. Most components are scheduled for delivery for assembly in the spring of 2010. The current estimate from FNAL is that the engineering run will take 15 weeks for chip fabrication and 12 weeks for testing at FNAL, which would make chips available for assembly onto wedges sometime in the March-April 2010 time frame. The current schedule float is 3 months, until December 2009. These time estimates do not include the time required to process the purchase requisition at BNL. There was also some discussion of the number of wafers to procure. Based on expected number of die per wafer and die yield, it is expected that a minimum of 10 wafers will be required. MOSIS guarantees a minimum number of good wafers but may deliver more in an engineering run. An order for 12 wafers may result in as many as 24 wafers depending on wafer yield. The consensus is that a total of 12 wafers should be ordered, with an expected price of $258K.

The reviewers want to thank the FVTX group for all the effort that they put into preparing for the review and the clear presentation of the testing done to date. Based on these results, it appears that the FPHX-2 chip functions as designed and is suitable for the PHENIX experiment. A couple of questions came up during the presentation, most notably on the features of some of the gain plots (slide 19, J. Kapustinsky) , and the reviewers would like to request that the FVTX group look closer into what cuts were applied to make sure that there are no problems with the some of the gain settings.

There were no results of testing of the leakage compensation circuit on the chip. This circuit is not required for AC operation, however; it might play a role if there is a problem with the AC coupling of the sensor to the FPHX chip. While there is no indication that there is no negative effect of the circuit for AC coupled sensors, the FVTX group should make a few studies to confirm that it does not effect operation for AC coupled sensors.

Some of the reviewers remain concerned about the zero ADC issue and that the explanation should be provided as part of the chip documentation. There is some feeling that this is a result of a time slewing issue in the chip that is not fully understood, and that when moving to larger scale production, it could create a problem. In order to makes sure that the timing of the detector is well understood, the FVTX group should prepare a timing block diagram indicating the timing spread allowances at each stage.

The feeling of the reviewers is that these issues are not sufficient to delay the fabrication of the chip. Given the schedule constraints and the need to construct a detector system in a timely manner, preparation for fabrication of the chip should proceed. Concurrent with that, the FVTX group should continue to test the chips that are currently available and documentation of the chip features and characterization testing should be completed.